

10/521941  
Rec'd R/PTO 21 JAN 2005

ABSTRACT OF THE DISCLOSURE

A protecting element, comprising a first n+-type region, an insulating region, and a second n+-type region, is connected in parallel between two terminals of an FET. Since discharge across the first and second n+ regions is enabled, electrostatic energy that reaches the operating region of the FET can be attenuated without increasing the parasitic capacitance.

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